enter the following amendments and consider the following remarks.

Specification Amendments

Please replace paragraph 004 with the following rewritten paragraph:

004 As device sizes decrease below 0.13 micron critical dimension, however, the gap fill of openings, for example STI openings, becomes problematical and the process window for successful gap filling is narrowed. Generally, as device sizes decrease and aspect ratios increase to greater than about 4 to 1, relatively high plasma RF powers, for example, greater than about 6 Watts/cm^2 are delivered to a process wafer surface creating relatively large thermal stresses during the gap filling deposition. To maintain lower deposition temperatures the backside of the wafer is frequently cooled, leading to increased thermal gradients and consequently stresses across the wafer surface and through the wafer thickness. Consequently,

compressive stresses, relatively larger parallel to the wafer process surface, are generated following the HDP-CVD process leading to subsequent problems in device quality and reliability. For example, charge carrier mobilities are strongly influenced, e.g., decreased due to stress fields present in semiconductor materials.

Please replace paragraph 006 with the following rewritten paragraph:

006 It is therefore among the objects of the present invention to provide an improved method for filling gaps including shallow trench isolation (STI) structures as well as forming a STI structure having reduced stresses to achieve improved semiconductor device quality and reliability, in addition to overcoming other shortcomings and deficiencies of the prior art.

Please replace paragraph 0027 with the following rewritten

paragraph:

0027 Referring to Figure 2C, in another embodiment, a plurality of trench filling layers are formed with one or more CVD USG layers, e.g., SACVD, APCVD, or HDPCVD, together with one or more SOG layers, with an optional annealing process performed between each layer deposition, but at least following deposition of the uppermost trench filling layer. For example, a first layer 28A of CVD USG or SOG (including a curing process) is deposited to about less than about 1/2, e.g., about 1/3 the depth of the trench by a first deposition using a CVD process or SOG process (including a curing process) followed by an annealing process according to preferred embodiments. A second layer 28B of CVD USG or SOG (including a curing process) is then deposited to about the same thickness followed by a second annealing process. A third layer e.g., 28C of CVD USG or SOG (including a curing process) is then deposited to a final thickness e.g., the deposited layers having a total thickness of from about 2000 to about 8000 Angstroms, followed by a third

annealing process. Preferably, a HDP-CVD process is used for only the second and subsequent deposited layers e.g., 28B, 28C layers following initial depositions e.g., first and second layers of SOG or APCVD or SACVD, to reduce the possibility of void formation. In addition, with multiple layers being formed of SOG oxide, SACVD oxide (USG) and/or APCVD oxide (USG), an annealing process between layer depositions may be optionally foregone, with the annealing process ~~be~~ carried out following deposition of the final oxide layer.

Please replace paragraph 0029 with the following rewritten paragraph:

0029 According to preferred embodiments for forming a reduced (relaxed) stress STI oxide filling, it has been found that MOSFET device performance is improved. For example, by reducing stresses in the length and width directions of the STI oxide, e.g., in the plane of (parallel) or perpendicular to the semiconductor substrate major surface, charge carrier mobility, including electrons and holes in N and PMOS devices,

respectively, is improved in adjacent semiconductor material portions. The improvement in charge carrier mobility shows improvement particularly in the case of subsequent formation of self aligned metal silicides (salicides), e.g., $CoSi_2$, NiSi, and $TiSi_2$, over source/drain regions of the semiconductor substrate, including e.g., silicon epitaxially grown (SEG) raised source/drain regions. For example referring to Figure 2D is shown an exemplary MOSFET device having STI regions 32A and 32B formed according to preferred embodiments in semiconductor substrate 12, followed by conventional processes to form S/D doped regions e.g., 34A, a polysilicon gate structure 36 with gate oxide 37, oxide and/or nitride spacers e.g., 38, SDE doped regions 34B, and salicide regions e.g., 36A, 36B, formed over raised S/D silicon epitaxial growth (SEG) regions e.g., 38A and 38B, as well as an upper portion of the polysilicon gate structure, e.g. 36C. The improved charge carrier mobility in the S/D regions adjacent the relaxed oxide filled STI structures 32A and 32B, for example, reduces sheet resistance, allowing shallower junction depths (e.g., SDE regions) to be formed, including raised S/D regions, improving device performance and

reliability. For example Id_{sat} is improved by improved charge carrier mobility enabled by relaxed oxide filled STI structures. It will be appreciated that the relaxed oxide filled STI structure formation process may be advantageously used with other device technologies including substrates including strained Si, silicon on insulator (SOI), and SiGe as well as the formation of advanced MOSFET structures such as finFET devices.